National Semiconductor

SPECIALTY Products CMOS EEPROM Selection Guide

General Description

National Semiconductor offers a full line of CMOS EEPROMs. Some share the MICROWIRE™ Serial Interface such as the NM93C06 and the NM93CS06; others share the I²C (2-wire) interface such as the NM24C02 and the NM24C08. In addition to the above EEPROMs, we also offer some specialty EEPROMs.

These include the NM95C12, NM93C46A and the NM25C04 EEPROMs.

Features

- No erase necessary
- MICROWIRE compatible interface
- Self-timed programming cycle
- 40 years data retention
- Endurance: 10^6 data changes
- Reliable CMOS floating gate technology

The **NM95C12** is a 976-bit CMOS EEPROM with 8 programmable outputs that can be used as switches, i.e., DIP or analog. The 976 bits of memory are divided into 61 registers of 16 bits each with each register individually accessible. Registers 61–63 are dedicated for DIP switch functions. The NM95C12 contains 8 individually programmable outputs which can be used as switches.

The **NM25C04** is 4096 bits of CMOS EEPROM with an SPI-interface. The device is designed to seamlessly interface with the 68HCXX family of Motorola microcontrollers.

The **NM93C46A** is 1024 bits of CMOS EEPROM which can be organized as either 64 16-bit registers or as 128 8-bit registers. The NM93C46A shares the MICROWIRE interface and the x8 and x16 configuration. The differentiating feature is in the pin configuration: The NM93C46A's Program/Erase status is output on the Data-Out (DO) pin. The device uses a low to high transition on the clock (SK) to clock all data into or out of the device, except device programming status which is independent of the clock.

Available Product

	Packages	Temperature Ranges	4.5V–5.5V	2.5V–5.5V
NM95C12	N, M	C, E	Y	
NM93C46A	N, M8	C, E	Y	Y
NM25C04	N, M	C, E		Y

National Semiconductor

NM93C06/C46/C56/C66
256-/1024-/2048-/4096-Bit Serial EEPROM (MICROWIRE™ Bus Interface)

General Description

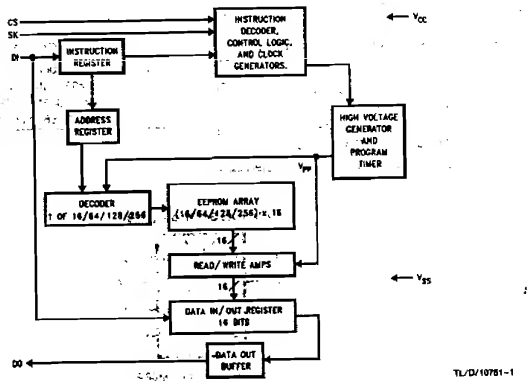
The NM93C06/C46/C56/C66 devices are 256/1024/2048/4096 bits, respectively, of CMOS non-volatile electrically erasable memory divided into 16/64/128/256 16-bit registers. They are fabricated using National Semiconductor's floating-gate CMOS process for high reliability and low power consumption. These memory devices are available in an SO package for small space considerations.

The EEPROM interfacing is MICROWIRE compatible for simple interface to standard microcontrollers and microprocessors. There are 7 instructions that control these devices: Read, Erase/Write Enable, Erase, Erase All, Write, Write All, and Erase/Write Disable. The ready/busy status is available on the DO pin during programming.

Features

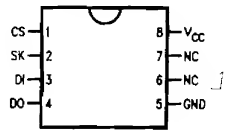
- Device status during programming mode
- Typical active current of 400 μA; Typical standby current of 25 μA
- No erase required before write
- Reliable CMOS floating gate technology
- 4.5V to 5.5V operation in all modes
- MICROWIRE compatible serial I/O
- Self-timed programming cycle
- 40 years data retention
- Endurance: 10^6 data changes
- Packages available: 8-pin SO, 8-pin DIP

Block Diagram



Connection Diagrams

Dual-In-Line Package (N) and 8-Pin SO (M8)



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Top View

See NS Package Number N08E and M08A

Pin Names

CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
V_{CC}	Power Supply

Ordering Information

Commercial Temp. Range (0°C to +70°C)

Order Number*
NM93C06N/NM93C46N
NM93C56N/NM93C66N
NM93C06M8/NM93C46M8
NM93C56M8/NM93C66M8

Extended Temp. Range (−40°C to +85°C)

Order Number*
NM93C06EN/NM93C46EN
NM93C56EN/NM93C66EN
NM93C06EM8/NM93C46EM8
NM93C56EM8/NM93C66EM8

*For 14-Pin SO availability contact your local National Semiconductor Sales Office.

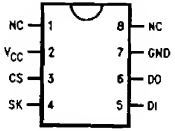
Alternate (Turned) SO Pinout

Order Number
NM93C06TM8/NM93C46TM8/NM93C56TM8
NM93C06TEM8/NM93C46TEM8/NM93C56TEM8

Military Temp. Range (−55°C to +125°C)

Order Number*
NM93C06MN/NM93C46MN
NM93C56MN/NM93C66MN
NM93C06MM8/NM93C46MM8
NM93C56MM8/NM93C66MM8

Alternate SO Pinout (TM8)



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See NS Package M08A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Ambient Storage Temperature	−65°C to +150°C
All Input or Output Voltages with Respect to Ground	+6.5V to −0.3V
Lead Temp. (Soldering, 10 sec.)	+300°C
ESD Rating	2000V

Operating Conditions

Ambient Operating Temperature	
NM93C06–NM93C66	0°C to +70°C
NM93C06E–NM93C66E	−40°C to +85°C
NM93C06M–NM93C66M	−55°C to +125°C
Power Supply (V_{CC})	4.5V to 5.5V

DC and AC Electrical Characteristics V_{CC} = 5.0V ± 10% unless otherwise specified

Note: Throughout this table, "M" refers to temperature range (−55°C to +125°C), not package.

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
I_{CCA}	Operating Current	NM93C06-NM93C66 NM93C06E-NM93C66E NM93C06M–NM93C66M	CS = V_{IH}, SK = 1 MHz SK = 1 MHz SK = 0.5 MHz		1 1 1	mA
I_{CCS}	Standby Current	NM93C06-NM93C66 NM93C06E-NM93C66E NM93C06M–NM93C66M	CS = V_{IL}		50 50 100	μA μA μA
I_{IL} I_{OL}	Input Leakage Output Leakage		V_{IN} = 0V to V_{CC} (Note 4)		±1	μA
V_{IL} V_{IH}	Input Low Voltage Input High Voltage			−0.1 2	0.8 V_{CC} + 1	V
V_{OL1} V_{OH1}	Output Low Voltage Output High Voltage		I_{OL} = 2.1 mA I_{OH} = −400 μA	 2.4	0.4	V V
V_{OL2} V_{OH2}	Output Low Voltage Output High Voltage		I_{OL} = 10 μA I_{OH} = −10 μA	 V_{CC} − 0.2	0.2	V
f_{SK}	SK Clock Frequency	NM93C06-NM93C66 NM93C06E-NM93C66E NM93C06M–NM93C66M	(Note 5)	0 0	 1 0.5	MHz
t_{SKH}	SK High Time	NM93C06-NM93C66 NM93C06E-NM93C66E NM93C06M–NM93C66M		250 300 500		ns
t_{SKL}	SK Low Time			250		ns
t_{SKS}	SK Setup Time		SK must be at V_{IL} for t_{SKS} before CS goes high	50		ns
t_{CS}	Minimum CS Low Time	NM93C06-NM93C66 NM93C06E-NM93C66E NM93C06M–NM93C66M	(Note 2)	250 250 500		ns

DC and AC Electrical Characteristics V_{CC} = 5.0V ± 10% (unless otherwise specified) (Continued)

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
t_{CSS}	CS Setup Time	NM93C06-NM93C66 NM93C06E-NM93C66E NM93C06M-NM93C66M		50 50 100		ns
t_{DH}	D0 Hold Time			70		ns
t_{DIS}	DI Setup Time	NM93C06-NM93C66 NM93C06E-NM93C66E NM93C06M-NM93C66M		100 200 200		ns
t_{CSH}	CS Hold Time			0		ns
t_{DIH}	DI Hold Time			20		ns
t_{PD1}	Output Delay to "1"	NM93C06-NM93C66 NM93C06E-NM93C66E NM93C06M-NM93C66M			500 500 1000	ns
t_{PD0}	Output Delay to "0"	NM93C06-NM93C66 NM93C06E-NM93C66E NM93C06M-NM93C66M			500 500 1000	ns
t_{SV}	CS to Status Valid	NM93C06-NM93C66 NM93C06E-NM93C66E NM93C06M-NM93C66M			500 500 1000	ns
t_{DF}	CS to DO in TRI-STATE®	NM93C06-NM93C66 NM93C06E-NM93C66E NM93C06M-NM93C66M	CS = V_{IL}		100 100 200	ns
t_{WP}	Write Cycle Time				10	ms

Capacitance (Note 3)

T_A = 25°C f = 1 MHz

Symbol	Test	Typ	Max	Units
C_{OUT}	Output Capacitance		5	pF
C_{IN}	Input Capacitance		5	pF

Note 1: Stress ratings above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: CS (Chip Select) must be brought low (to V_{IL}) for an interval of t_{CS} in order to reset all internal device registers (device reset) prior to beginning another opcode cycle. (This is shown in the opcode diagrams in the following pages).

Note 3: This parameter is periodically sampled and not 100% tested.

Note 4: Typical leakage values are in the 20 nA range.

Note 5: The shortest allowable SK clock period = $1/f_{SK}$ (as shown under the f_{SK} parameter). Maximum SK clock speed (minimum SK period) is determined by the interaction of several AC parameters stated in the datasheet. Within this SK period, both t_{SKH} and t_{SKL} limits must be observed. Therefore, it is not allowable to set $1/f_{SK} = t_{SKminimum} + t_{SKLminimum}$ for shorter SK cycle time operation.

AC Test Conditions

V_{CC} Range	V_{IL}/V_{IH} Input Levels	V_{IL}/V_{IH} Timing Level	V_{OL}/V_{OH} Timing Level	I_{OL}/I_{OH}
4.5V ≤ V_{CC} ≤ 5.5V (TTL Levels)	0.4V/2.4V	1.0V/2.0V	0.4V/2.4V	−2.1 mA/0.4 mA

Output Load: 1 TTL Gate (C_L = 100 pF)

Functional Description

The NM93C06/C46/C56/C66 devices have 7 instructions as described below. Note that the MSB of any instruction is a "1" and is viewed as a start bit in the interface sequence. For the C06 and C46 the next 8 bits carry the op code and the 6-bit address for register selection. For the C56 and C66 the next 10-bits carry the op code and the 8-bit address for register selection.

All Data in signals are clocked into the device on the low-to-high SK transition.

Read (READ):

The READ instruction outputs serial data on the DO pin. After a READ instruction is received, the instruction and address are decoded, followed by data transfer from the selected memory register into a 16-bit serial-out shift register. A dummy bit (logical 0) precedes the 16-bit data output string. Output data changes are initiated by a low to high transition of the SK clock.

Erase/Write Enable (WEN):

When V_{CC} is applied to the part, it powers up in the Erase/Write Disable (WDS) state. Therefore, all programming modes must be preceded by an Erase/Write Enable WEN instruction. Once an Erase/Write Enable instruction is executed, programming remains enabled until an Erase/Write Disable (WDS) instruction is executed or V_{CC} is completely removed from the part.

Erase (ERASE):

The ERASE instruction will program all bits in the selected register to the logical '1' state. CS is brought low following the loading of the last address bit. This falling edge of the CS pin initiates the self-timed programming cycle.

The DO pin indicates the READY/BUSY status of the chip if CS is brought high after the t_{CS} interval. DO = logical '0' indicates that programming is still in progress. DO = logical '1' indicates that the register, at the address specified in the instruction, has been erased, and the part is ready for another instruction.

Write (WRITE):

The WRITE instruction is followed by 16 bits of data to be written into the specified address. After the last bit of data is put on the data-in (DI) pin, CS must be brought low before the next rising edge of the SK clock. This falling edge of CS initiates the self-timed programming cycle. The DO pin indicates the READY/BUSY status of the chip if CS is brought high after the t_{CS} interval. DO = logical 0 indicates that programming is still in progress. DO = logical 1 indicates that the register at the address specified in the instruction has been written with the data pattern specified in the instruction and the part is ready for another instruction.

Erase All (ERAL):

The ERAL instruction will simultaneously program all registers in the memory array and set each bit to the logical '1' state. The Erase All cycle is identical to the ERASE cycle except for the different op-code. As in the ERASE mode, the DO pin indicates the READY/BUSY status of the chip if CS is brought high after the t_{CS} interval.

Write All (WRALL):

The WRALL instruction will simultaneously program all registers with the data pattern specified in the instruction. As in the WRITE mode, the DO pin indicates the READY/BUSY status of the chip if CS is brought high after the t_{CS} interval.

Write Disable (WDS):

To protect against accidental data disturb, the WDS instruction disables all programming modes and should follow all programming operations. Execution of a READ instruction is independent of both the WEN and WDS instructions.

NOTE: The NSC CMOS EEPROMs do not require an 'ERASE' or 'ERASE ALL' operation prior to the 'WRITE' and 'WRITE ALL' instructions. The 'ERASE' and 'ERASE ALL' instructions are included to maintain compatibility with earlier technology EEPROMs.

Instruction Set for the NM93C06 and NM93C46

Instruction	SB	Op Code	Address	Data	Comments
READ	1	10	A5–A0		Reads data stored in memory, at specified address.
WEN	1	00	11XXXX		Enable all programming modes.
ERASE	1	11	A5–A0		Erase selected register.
WRITE	1	01	A5–A0	D15–D0	Writes selected register.
ERAL	1	00	10XXXX		Erases all registers.
WRALL	1	00	01XXXX	D15–D0	Writes all registers.
WDS	1	00	00XXXX		Disables all programming modes.

Note: Address bits A5 and A4 become "Don't Care" for the NM93C06.

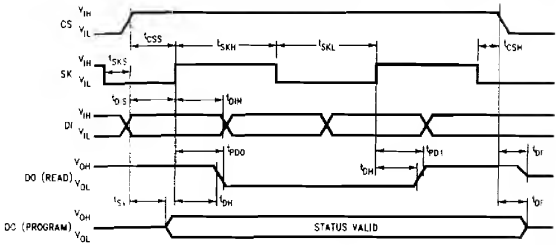
Instruction Set for the NM93C56 and NM93C66

Instruction	SB	Op Code	Address	Data	Comments
READ	1	10	A7–A0		Reads data stored in memory, at specified address
WEN	1	00	11XXXXXX		Enable all programming modes.
ERASE	1	11	A7–A0		Erase selected register.
ERAL	1	00	10XXXXXX		Erases all registers.
WRITE	1	01	A7–A0	D15–D0	Writes selected register.
WRALL	1	00	01XXXXXX	D15–D0	Writes all registers.
WDS	1	00	00XXXXXX		Disables all programming modes.

Note: Address bit A7 becomes "Don't Care" for the NM93C56.

Timing Diagrams

Synchronous Data Timing



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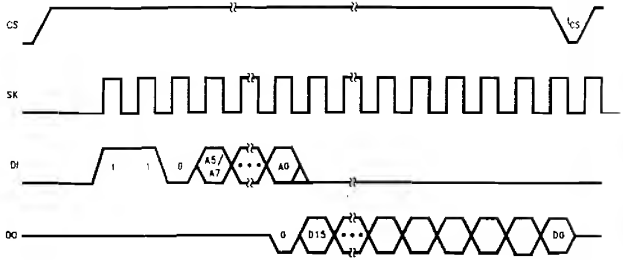
READ



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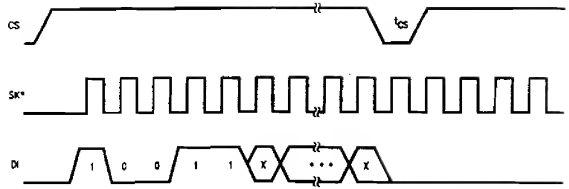
WEN



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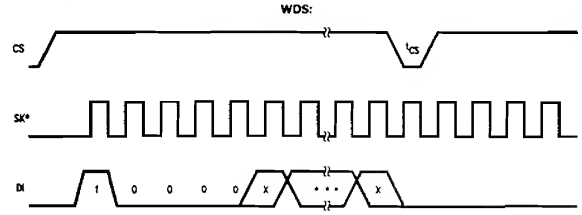
Timing Diagrams (Continued)

WDS:



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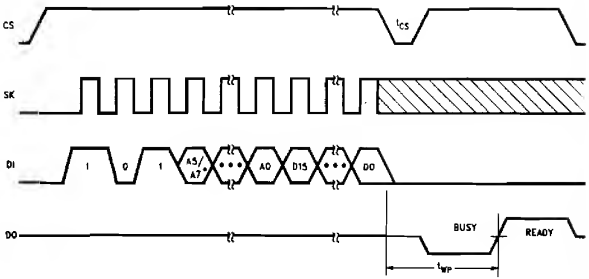
WRITE:



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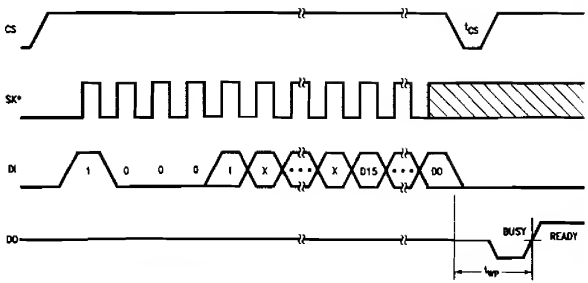
WRALL:



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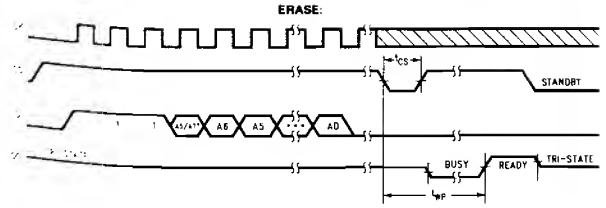
ming Diagrams (Continued)

ERASE:



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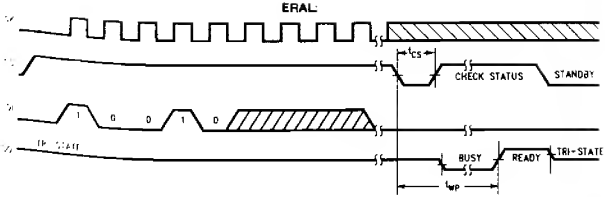
ERAL:



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National Semiconductor

NM93CS06/CS46/CS56/CS66 (MICROWIRE™ Bus Interface) 256-/1024-/2048-/4096-Bit Serial EEPROM with Data Protect and Sequential Read

General Description

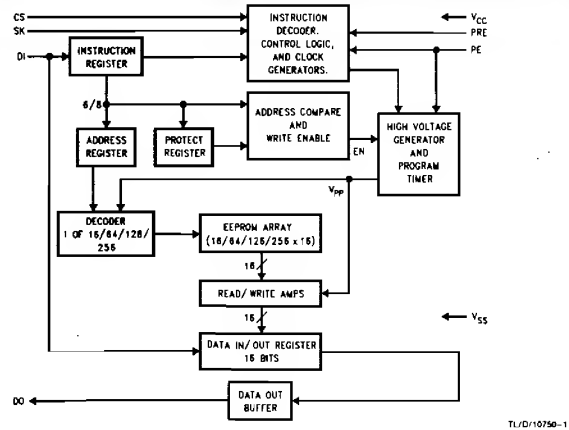
The NM93CS06/CS46/CS56/CS66 devices are 256/1024/2048/4096 bits, respectively, of CMOS non-volatile electrically erasable memory divided into 16/64/128/256 16-bit registers. Selected registers can be protected against data modification by programming the Protect Register with the address of the first register to be protected against data modification (all registers greater than, or equal to, the selected address are then protected from further change). Additionally, this address can be "locked" into the device, making all future attempts to change data impossible. These devices are fabricated using National Semiconductor floating-gate CMOS process for high reliability, high endurance and low power consumption. The NM93CSXX Family is offered in an SO package for small space considerations.

The EEPROM interfacing is MICROWIRE compatible providing simple interfacing to standard microcontrollers and microprocessors. There are a total of 10 instructions, 5 which operate on the EEPROM memory, and 5 which operate on the Protect Register. The memory instructions are READ, WRITE, WRITE ALL, WRITE ENABLE, and WRITE DISABLE. The Protect register instructions are PRREAD, PRWRITE, PRENABLE, PRCLEAR, and PRDISABLE.

Features

- Write protection in a user defined section of memory
- Sequential register read
- Typical active current of 400 μA and standby current of 25 μA
- No erase required before write
- Reliable CMOS floating gate technology
- MICROWIRE compatible serial I/O
- Self timed write cycle
- Device status during programming mode
- 40 year data retention
- Endurance: 10^6 data changes
- 4.5V to 5.5V operation in all modes of operation
- Packages available: 8-pin SO, 8-pin DIP

Block Diagram



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